ABSTRACT OF THE DISCLOSURE

A port A of the path including a first transistor of a memory cell to be accessed, a first bit line pair, a first column selection switch and a data line pair interleaves with a port B of the path including a second transistor of the memory cell to be accessed, a second bit line pair, a second column selection switch and the data line pair in two cycles of a clock. A read amplifier amplifies data transferred from a bit line pair to the data line pair and outputs the resultant data to an input/output buffer in one cycle of the clock. The input/output buffer outputs the data received from the read amplifier to the outside in one cycle of the clock.